AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claims 1-4 (canceled).

5. (currently amended) ~~The~~ A semiconductor integrated circuit ~~according to claim 4, comprising:~~ wherein an analog circuit operating in response to a first clock signal and a digital circuit operating in response to a second clock signal having the same period as that of the first clock signal are formed on the same semiconductor substrate; comprising on the semiconductor substrate:

a plurality of phase shift circuits each relatively shifting a phase of one of the first clock signal and the second clock signal from a phase of the other of the first clock signal and the second clock signal by a different value;

a noise measuring circuit for measuring a noise component generated by the analog circuit,

wherein the noise component is measured during a manufacturing stage;

selection control means for successively replacing and selecting the plurality of phase shift circuits during the manufacturing stage;

phase shift setting means for obtaining a minimum value out of the noise components measured when each of the phase shift circuits is selected and setting a phase shift value by fixedly selecting only a phase shift circuit selected when the noise component assumes the minimum value;

operation start control means for starting an operation of the selection control means when a first specified time elapses after having powered on; and

time measuring means for measuring a second specified time after termination of successive selection of the phase shift circuits by the selection control means, and operating the selection control means when the second specified time elapses, wherein

successive selection of the phase shift circuits is repeated at intervals of the second specified time.

6. (currently amended) ~~The~~ A semiconductor integrated circuit ~~according to claim 2,~~ wherein an analog circuit operating in response to a first clock signal and a digital circuit operating in response to a second clock signal having the same period as that of the first clock signal are formed on the same semiconductor substrate; comprising on the semiconductor substrate:

a plurality of phase shift circuits each relatively shifting a phase of one of the first clock signal and the second clock signal from a phase of the other of the first clock signal and the second clock signal by a different value;

a noise measuring circuit for measuring a noise component generated by the analog circuit,

wherein the noise component is measured during a manufacturing stage;

selection control means for successively replacing and selecting the plurality of phase shift circuits during the manufacturing stage; and

phase shift setting means for obtaining a minimum value out of the noise components measured when each of the phase shift circuits is selected and setting a phase shift value by fixedly selecting only a phase shift circuit selected when the noise component assumes the minimum value

wherein

the analog circuit is a solid-state image sensing element array; and

the noise component measured by the noise measuring circuit is a noise component superimposed on a video signal of a shielded region outputted from the solid-state image sensing element array during one valid horizontal period; and

successive selection of the phase shift circuits by the selection control means is performed in synchronization with a vertical period.